PVP 20

Code: 20IT3402

II B.Tech - II Semester – Regular Examinations – JULY 2022

COMPUTER ORGANIZATION
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

UNIT – I

1. a) Discuss one stage of arithmetic logic shift unit with neat sketch. 7 M
   b) Draw the 4 bit arithmetic circuit. 7 M

OR

2. a) Describe Three state bus buffer with neat sketch. 7 M
   b) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.
   xyT0 + T1 + y' T2: AR ←AR+1 7 M

UNIT – II

3. a) List the Registers for the Basic Computer and mention the purposes of registers. 7 M
   b) A digital computer has a memory unit with a capacity of 16348 units, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part. Two instructions are packed in

one memory word and a 40 bit Instruction Register (IR) is available in the control unit. Formulae a procedure for fetching and executing instructions for this computer. 7 M

OR

4. a) The control unit determines the type of instruction that was just read from memory. Draw the flow chart and discuss how the control determines the instruction type after the decoding. 7 M

   b) Illustrate various phases of an instruction cycle with flow chart. 7 M

UNIT-III

5. a) Explain Data transfer, Data manipulation and Program control instructions with suitable examples. 10 M

   b) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated? 4 M

OR

6. a) A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is, 10 M

i. direct
ii. indirect
iii. relative
iv. indexed.

b) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is (i) a computational type requiring an operand from memory; (ii) a branch type. 4 M

UNIT – IV

7. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers.
i. (+ 12) * (+ 10)
ii. (+ 10) * (- 18) 14 M

OR

8. Describe in detail about Cache Mapping Techniques. 14 M

UNIT – V

9. a) Describe Asynchronous data transfer in detail. 4 M

b) Discuss the major difficulties that cause the instruction pipeline conflicts. 10 M

OR

10. a) Illustrate asynchronous data transfer with Handshaking method. 7 M

b) Explain Parallel Processing in detail. 7 M